PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	AMG/18/10644
1.3 Title of PCN	Additional wafer fab in ST Ang Mo Kio (Singapore) for PMOSFET products
1.4 Product Category	See product list
1.5 Issue date	2018-02-09

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Lorenzo NASO
2.1.2 Marketing Manager	Marcello SAN BIAGIO
2.1.3 Quality Manager	Jean-Marc BUGNARD

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Wafer fabrication	Catania CT6, Ang Mo Kio AMK6

4. Description of change		
	Old	New
4.1 Description	SG20 die in PMOS technology, embedded in STEF05PUR commercial product, is manufactured in Catania (Italy) wafer fab	SG20 die in PMOS technology, embedded in STEF05PUR commercial product, is manufactured in Catania (Italy) wafer fab and in Ang Mo Kio (Singapore). Catania fab will stop production of PMOSFET from H2 2018
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No impact	

5. Reason / motivation for change	
5.1 Motivation	ST Ang Mo Kio will be validated as an additional wafer fab for PMOSFET products in order to provide more flexibility in term of production and prepare the termination of the production of these products in ST Catania (Italy).
5.2 Customer Benefit	MANUFACTURING FLEXIBILITY

6. Marking of parts / traceability of change	
6.1 Description	New Finished Good codes

7. Timing / schedule	
7.1 Date of qualification results	2017-12-19
7.2 Intended start of delivery	2018-05-07
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	10644 REL-6088-410-W-17-STEF05PUR - UW70.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2018-02-09

9. Attachments (additional documentations)
10644 Public product.pdf 10644 REL-6088-410-W-17-STEF05PUR - UW70.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	STEF05DPUR	
	STEF05PUR	
	STEF05WPUR	

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Reliability Report

On

Change Process:

Qualification of SG20 with diffused in Ang Mo Kio.

TV: STEF05PUR

General Information	
Product Line	UW7001
Product Description	Electronic fuse for 5 V line
P/N	STEF05PUR
Product Group	AMS
Product division	POWER MANAGEMENT
Package	VDFPN 3x3x1.0 10 PITCH 0.50
Silicon Process technology	PMOSFET PP + BCD3S

Locations	
Wafer fab	SG20 AMK6 Singapore *UW70* AMK6 Singapore
Assembly plant	CARSEM China
Reliability Lab	Catania Reliability Lab
Reliability assessment	Pass

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	Dec-2017	6	Vito Gisabella	Giovanni Presti	Final Report

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

The STEF05 is an integrated electronic fuse optimized for monitoring output current and input voltage.

3.1 Objectives

VIPOWER transfer from CT6 to AMK

Reliability Qualification of SG20 line diffused in AMK6.

3.2 Test vehicle

STEF05PUR (Double Die SG20+UW70)

3.3 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

Electronic fuse for 5 V line

The STEF05 is an integrated electronic fuse optimized for monitoring output current and input voltage. Connected in series to a 5 V rail, it is capable of protecting the electronic circuitry on its output from overcurrent and overvoltage. The device has a controlled delay and turn-on time. When an overload condition occurs, the STEF05 limits the output current to a predefined safe value. If the anomalous overload condition persists, it goes into an open state, disconnecting the load from the power supply. If a continuous short-circuit is present on the board, when power is re-applied the E-fuse initially limits the output current to a safe value, and then again goes into an open state.

4.2 Construction note

	STEF05PUR	
Wafer/Die fab. information	**Die 1 – SG20**	**Die 2 - UW70**
Wafer fab manufacturing location	SINGAPORE AMK6	
Technology	PMOSFET SG20	BCD3S
Die finishing back side	Ti-Ni-Au	RAW SILICON
Die size	1650 x 890 micron	1700 x 1140 micron
Passivation type	TEOS + SiN	USG-PSG-SiON-PIX
Wafer Testing (EWS) information		
Electrical testing manufacturing location	Ang Mo Kio EWS	
Tester	ASL1K	
Tester Program	UW70_REV4_0.ZIP on PUW70AD6	
Assembly information		
Assembly site	CARSEM China	
Package description	VDFPN 3x3x1.0 10 PITCH 0.50	
Molding compound	Epoxy	
Frame material	P/N #442690SAM DFN 3X3 10L 104X75 RT-PPF	
Die attach material	Epoxy	
Wires bonding materials/diameters	1mil Cu wire - 2mil Cu wire	
Final testing information		
Testing location	Carsem China	
Tester	ASL1K	
Test program	STEF05_REV5_2.PRG	

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Package	Comments
1	VDFPN 3x3x1.0 10 PITCH 0.50	STEF05PUR (Double Die SG20+UW70)
2		
3		

5.2 Test plan and results summary

STEF05PUR

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						1°lot	2°lot	3°lot	
Die Oriented Tests									
HTS	N	JESD22 A-103	Ta = 150°C		168 H	0/45	0/45	0/45	
					500 H	0/45	0/45	0/45	
					1000 H	0/45	0/45	0/45	
HTS	N	JESD22 A-103	Ta = 175°C		168 H	0/45	0/45	0/45	Eng. evaluation
					500 H	0/45	0/45	0/45	
					1000 H	0/45	0/45	0/45	
HTOL	N	JESD22 A-108	Ta = 125°C, Vcc=+10V		168 H	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	
Package Oriented Tests									
PC		JESD22 A-113	Drying 24 H @ 125°C Store 40 H @ Ta=60°C Rh=60% Oven Reflow @ Tpeak=260°C 3 times		Final	pass	pass	pass	Go no go
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96H	0/77	0/77	0/77	
					168 H	0/77	0/77	0/77	Eng. evaluation
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	0/77	0/77	0/77	
					200 cy	0/77	0/77	0/77	
					500 cy	0/77	0/77	0/77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, Vcc=+7V		168 H	0/77	0/25	0/25	
					500 H	0/77	0/25	0/25	
					1000 H	0/77	0/25	0/25	
Other Tests									
ESD	N	ESDA/JEDEC JS 001	HBM	3	+/- 1500V +/- 2000V	PASS			
		ESDA/JEDEC JS 002	CDM	3	+/- 500V +/- 750V	PASS			+/- 750V Corner Pins

5.3 Tests Description

Test name	Description	Purpose
Die Oriented		
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
HTOL High Temperature Operative Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other Tests		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CDM: Charged Device Model HBM: Human Body Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.